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FIBOCOM UART Design Application Note

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Applicability Type

No.	Type	Note
1	All models	

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Versions

Version	Author	Assessor	Approver	Update Date	Description
V1.0.0				2013-08-13	Initial Version
V1.0.1				2015-04-26	Update the description of copyright and attention
V1.0.2				2015-08-24	Update the logo
V1.0.3				2017-05-23	Add 4 line serial port
V1.0.4	Wang Yuanguang	Liu Ke	Liu Ke	2018-12-06	Modify level conversion

Contents

1 UART Introduction 5

2 UART Interface Design 6

2.1 8 Wire UART 6

2.1.1 Direct Connection 6

2.1.2 Cross 7

2.2 2 Wire UART 8

2.3 Host UART 9

2.4 Interface Level 9

2.5 Level Conversion Design 10

2.5.1 Module Communicates with PC 10

2.5.2 Module Communicates with AP 11

2.6 Signal Integrity Design Requirements 12

2.6.1 TXD_N, RXD_N, CTS_N, RTS_N Wave Form 12

2.6.2 RING_N, DCD_N, DTR_N Control Signal 15

3 UART Software Design 16

4 Glossary 18

1 UART Introduction

The UART interface and interface level specification of Fibocom communication modules:

No.	Model No.	Interface Type	Interface Level(VDD)	Connection with DTE	Remarks
1	G600	A 8 wire serial bus interface	2.85V	Direct connection	
2	G610	A 8 wire serial bus interface	2.85V	Direct connection	
3	G620	A 8 wire serial bus interface	2.85V	Direct connection	
4	G510	A 8 wire serial bus interface Two 2 wire serial bus interface(Host UART, UART2)	2.85V	Cross	Host UART is used for downloading and debug. UART2 supports certain AT commands.
5	G520	A 6 wire serial bus interface(no UART1_DCD, UART1_RING) A 2 wire serial bus interface(Host UART)	2.85V	Cross	Host UART is used for downloading and debug.
6	H330-LGA	A 8 wire serial bus interface A 2 wire serial bus interface	1.8V	Cross	
7	H300-mini PCIe	A 7 wire serial bus interface (no UART1_DSR)	3.3V	Cross	

2 UART Interface Design

2.1 8 Wire UART

As the pin definitions are different for different modules, it includes direct connection and cross.

2.1.1 Direct Connection

The 8 wire serial bus interface is also called full serial bus interface, it is used for AT commands, GPRS data transmission, software upgrade and so on.

Pin definition:

No.	Pin Name	Description	Remarks
1	RXD_N	Module Received Data	DTE received data
2	TXD_N	Module Transmitted Data	DTE transmitted data
3	RING_N	Ring Indicator	Module notice DTE called
4	DSR_N	Data Set Ready	Module was ready
5	RTS_N	Request to Send	DTE notice module to send
6	DTR_N	Data Terminal Ready	DTE was ready
7	CTS_N	Clear to Send	Module switch to receive mode
8	DCD_N	Data Carrier Detect	Module notice DTE that Data Carrier was online

Note: The module is defined as DCE; application board is defined as DTE.

Reference design:

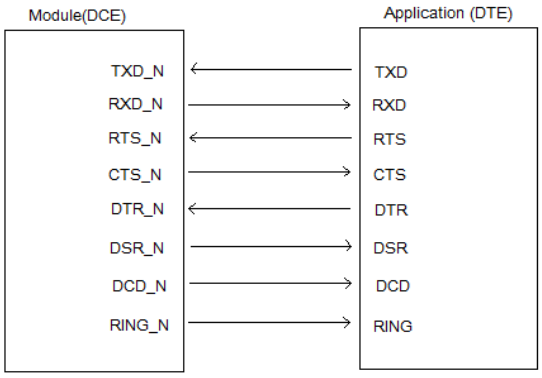

Figure 2-1 Reference Design

2.1.2 Cross

Pin definition:

No.	Pin Name	Description	Remarks
1	UART1_TXD	Module transmitted data	
2	UART1_RXD	Module received data	
3	UART1_CTS	Clear to Send	Module switch to receive mode
4	UART1_RTS	Request to Send	Module notice DTE to receive
5	UART1_DTR	Data Terminal Ready	DTE was ready
6	UART1_DSR	Data Set Ready	Module was ready
7	UART1_RING	Ring indicator	Module notice DTE get through
8	UART1_DCD	Data Carrier Detect	Module notice DTE that Data Carrier was online

Note: The module is defined as DCE; application board is defined as DTE.

Reference design:

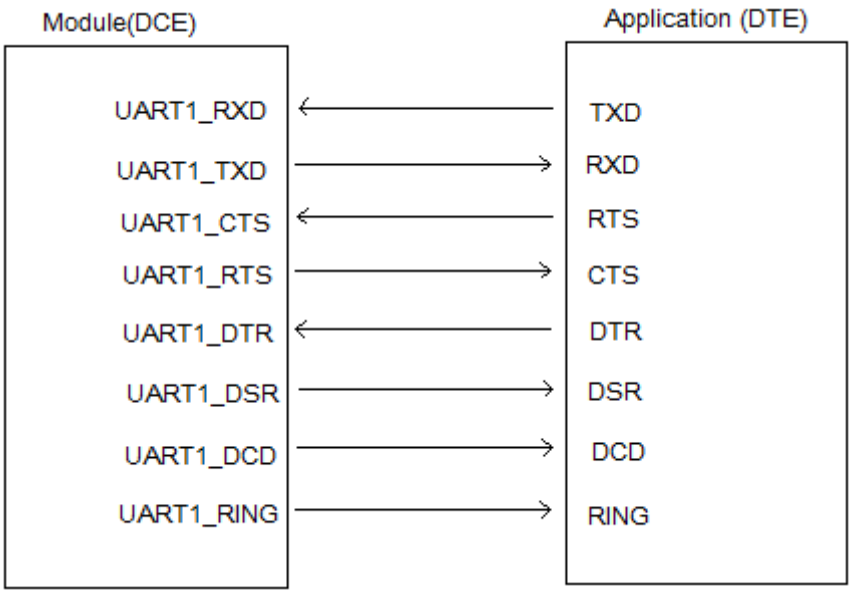

Figure 2-2 Reference Design

The UART supports hardware flow control and non-hardware flow control.

The default setting is 8 data bits, 1 stop bit and no parity.

In practice, in order to save the interface, 8 wires UART1 can use 2 wires (TXD\RXD), leave the other pin not connected. If you need flow control, please use RTS; if you need sleep mode, please use DTR.

2.2 4 Wire UART

The principle of pin signal definition varies with the module type.

2.2.1 Serial port design - crossover

Pin description is shown in the following table:

No.	Pin Name	Description	Remarks
1	UART1_TXD	Module Transmitted Data	
2	UART1_RXD	Module Received Data	
3	UART1_CTS	Clear to Send	Module switch to receive mode
4	UART1_RTS	Request to Send	Module notice DTE to receive

The reference design of 4-wire serial port (crossover) is as follows：

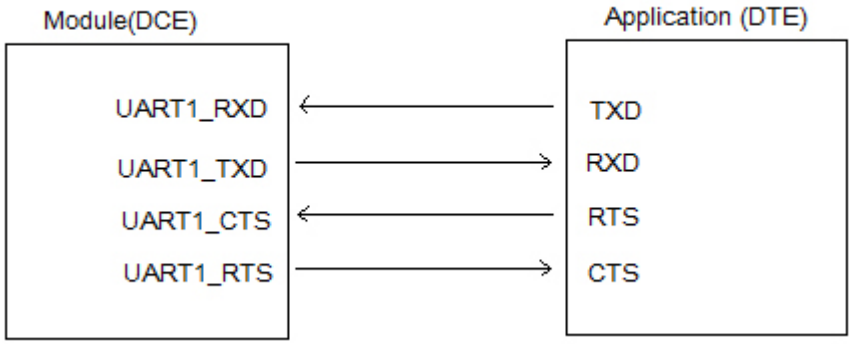

Figure2-3 Reference design of 4 serial port

Serial port supports hardware flow control or non-flow control.

The default port is configured with 8 data bits, 1 stop bit, and no parity.

In the module design application, in order to save the customer interface, 4-line UART1 can only use 2-line (TXD, RXD) to realize the communication function, and other pins can be suspended.However, RTS control is required for flow control.

2.3 2 Wire UART

The 2 wire serial bus interface only support some commands, for details, please refer to the AT commands User Manual.

Pin definition:

No.	Pin Name	Description
1	UART2_TXD	Module transmitted data
2	UART2_RXD	Module received data

Reference design (cross):

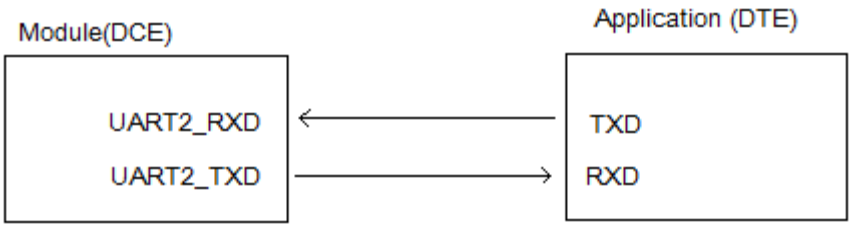

Figure 2-3 Reference Design

Note: UART2 only supports normal query function.

2.4 Host UART

Host UART is used for debugging, downloading, calibration, trace and so on, it doesn't support AT commands.

This port is used for debugging, only need to connect to test point.

Pin definition:

No.	Pin Name	Description
1	HST_RXD	Module received data
2	HST_TXD	Module transmitted data

Reference design:

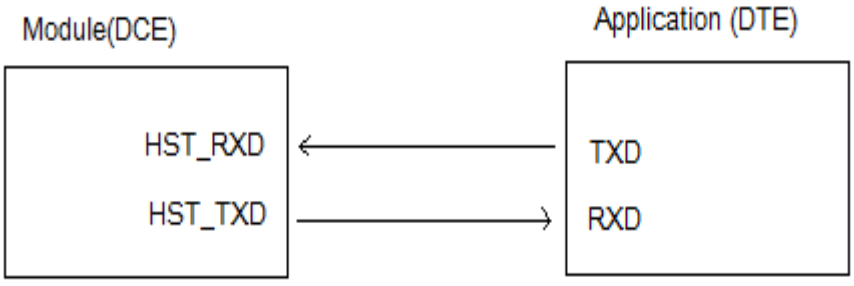

Figure 2-4 Reference Design

2.5 Interface Level

The following table shows the interface level:

Parameter	Description	Min.	Max.	Unit
VIL	Input, low level	-0.2	0.3*VDD	V
VIH	Input, high level	0.7*VDD	VDD+0.35	V
VOL	Output, low level	-0.2	0.35	V
VOH	Output, high level	VDD-0.2	VDD	V

Note: VDD is the power supply level for module; it is decided by the module number.

If the DTE interface level and module doesn't match, please add level conversion circuit.

2.6 Level Conversion Design

2.6.1 Module Communicates with PC

PC serial port level:

Level	Transmitter capable (V)	Receiver capable (V)
Logic 0	+5~+15	+3~+25
Logic 1	-5~-15	-3~-25

When module communicates with PC, it needs level conversion; the commonly used chips are SP3238E, MAX3221, PL2303 and so on.

The following figure shows the level conversion circuit when PC connects to module UART:

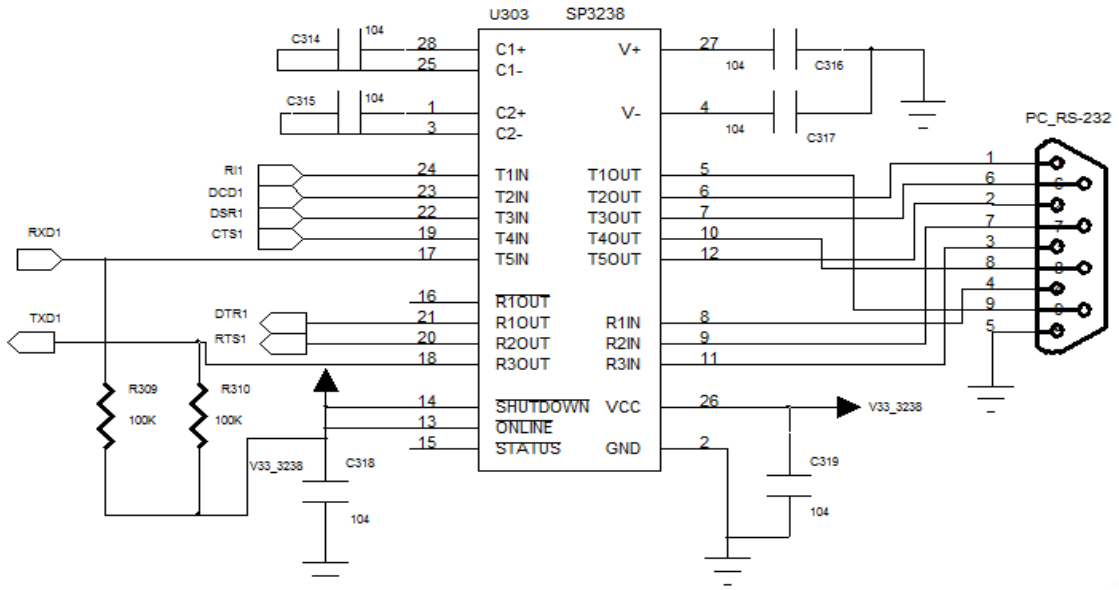

Figure 2-5 Level Conversion Circuit

2.6.2 Module Communicates with AP

When the DTE UART logic level and module UART level are different, please add level conversion.

The commonly used chips are 74LVC245, AN240, NC7WZ07 and so on; you can also use transistor or MOS as level conversion circuit.

When the terminal CPU UART level is in the range of 2.8V-3.3V, you can connect module to DTE CPU UART signal line with a 22ohm resistance.

When the terminal CPU UART level is lower than 2.8V or higher than 3.3V, please use level conversion circuit.

The following figure shows the DTE UART level conversion circuit:

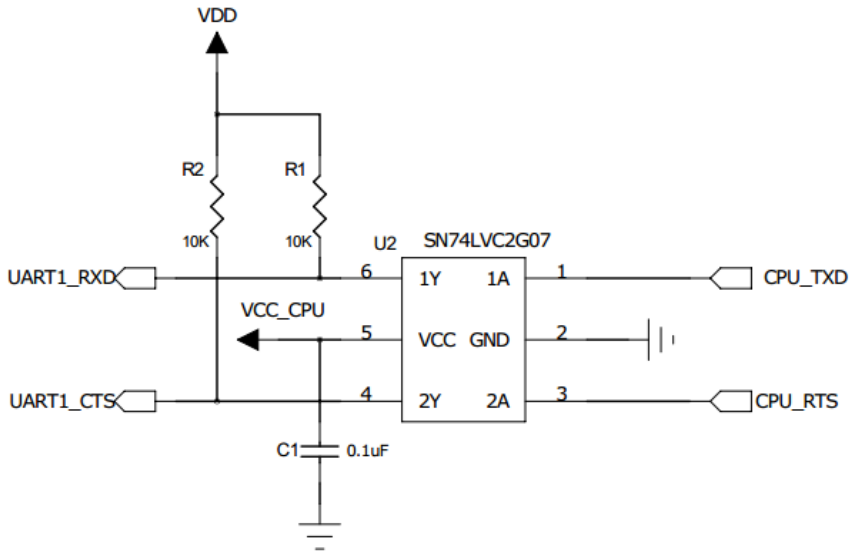

Figure 2-6 DTE UART level conversion circuit

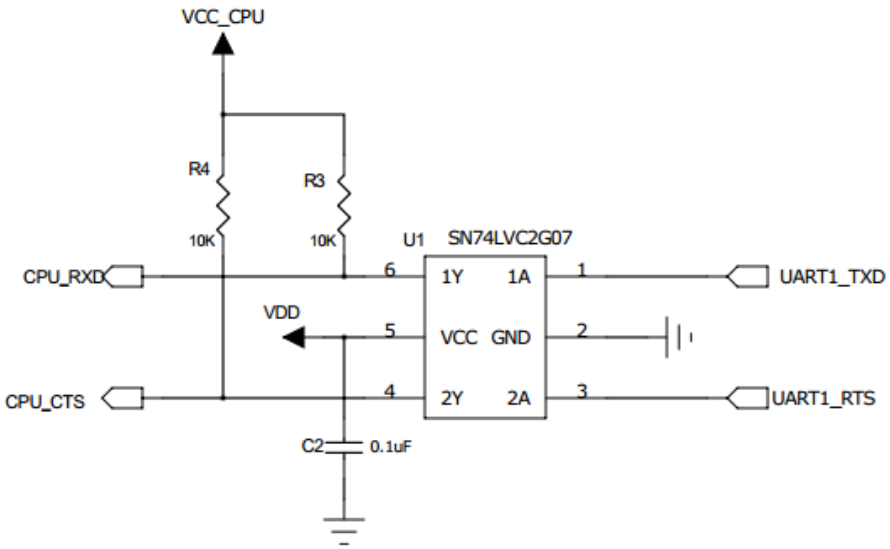

Figure 2-7 DTE UART level conversion circuit

Or you can use transistor to convert the level, as shown in the following figure:

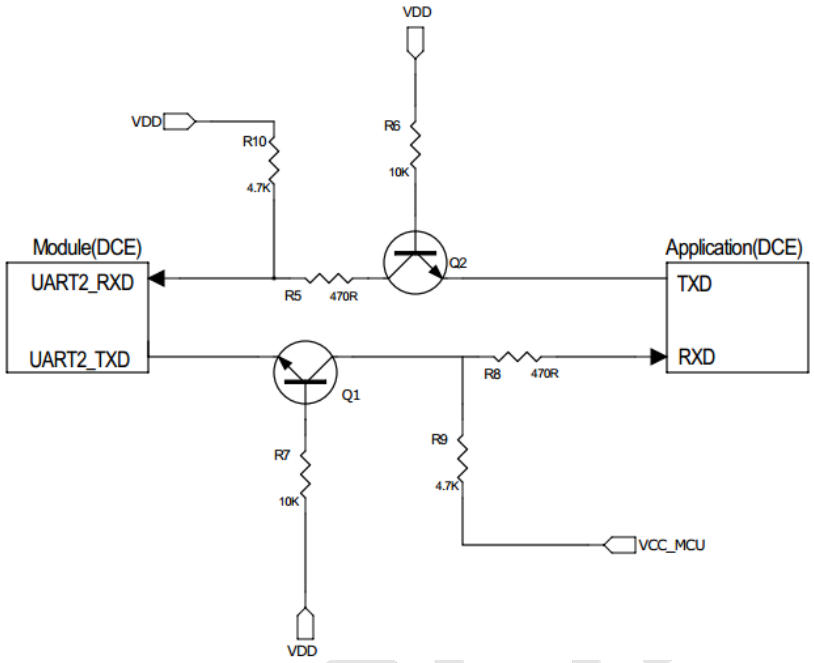

Figure 2-8 Transistor Level Conversion Circuit

2.7 Signal Integrity Design Requirements

2.7.1 TXD_N, RXD_N, CTS_N, RTS_N Wave Form

1. The following figure shows the wave form of TXD_N and RXD_N when the baud rate is 115200:

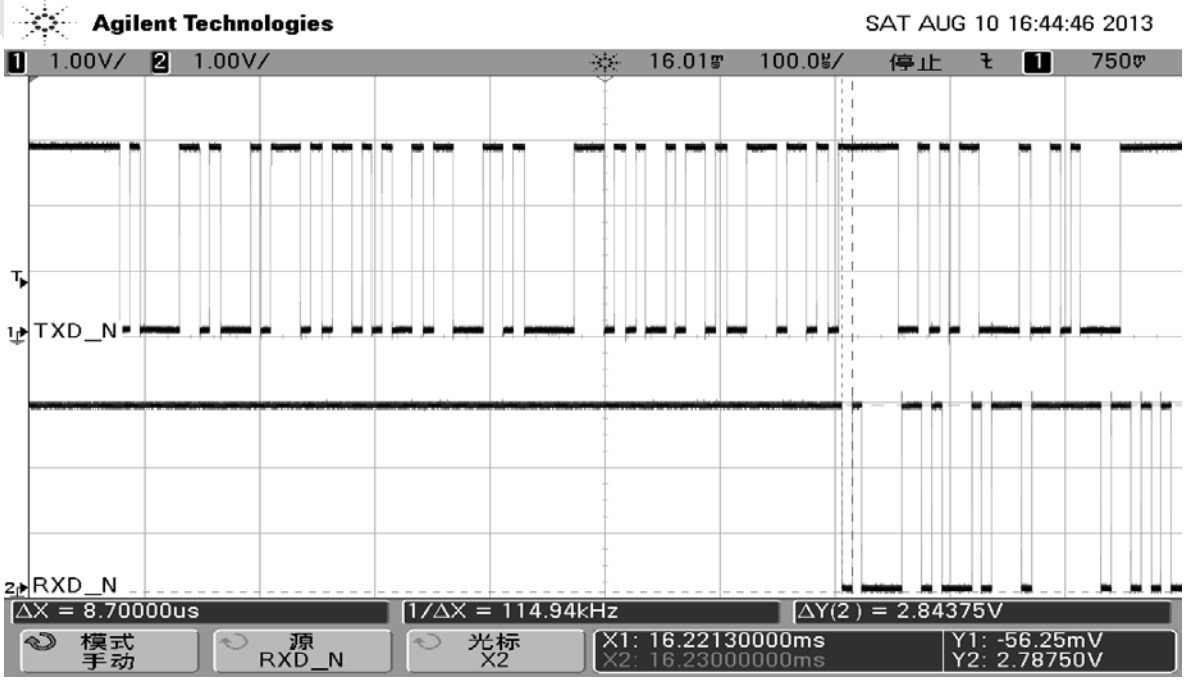

Figure 2-9 the wave form of TXD_N and RXD_N if you send AT command (baud rate is 115200)

2. By default, module is non-flow control (AT+IFC=0,0), CTS is low level, the level inputs by RTS_N doesn't affect TXD_N, RXD_N to transmitted data. As shown in the following figure:

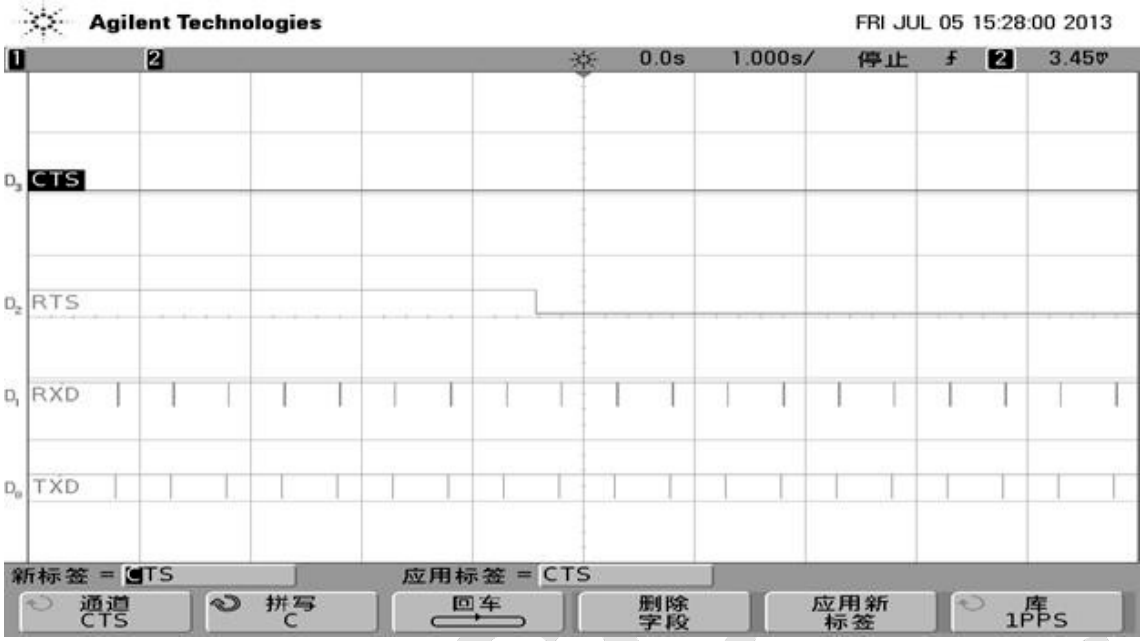

Figure 2-10 Wave Form

3. When the module is set to hardware flow control (AT+IFC=2,2), RTS_N inputs high level, RXD_N doesn't transmitted data, RTS_N inputs low level, RXD_N transmitted data (if there is no external DTE CPU input for RTS_N, high level output; if the external CPU controls signal, low level signal request the module to transmitted data). As shown in the following figure:

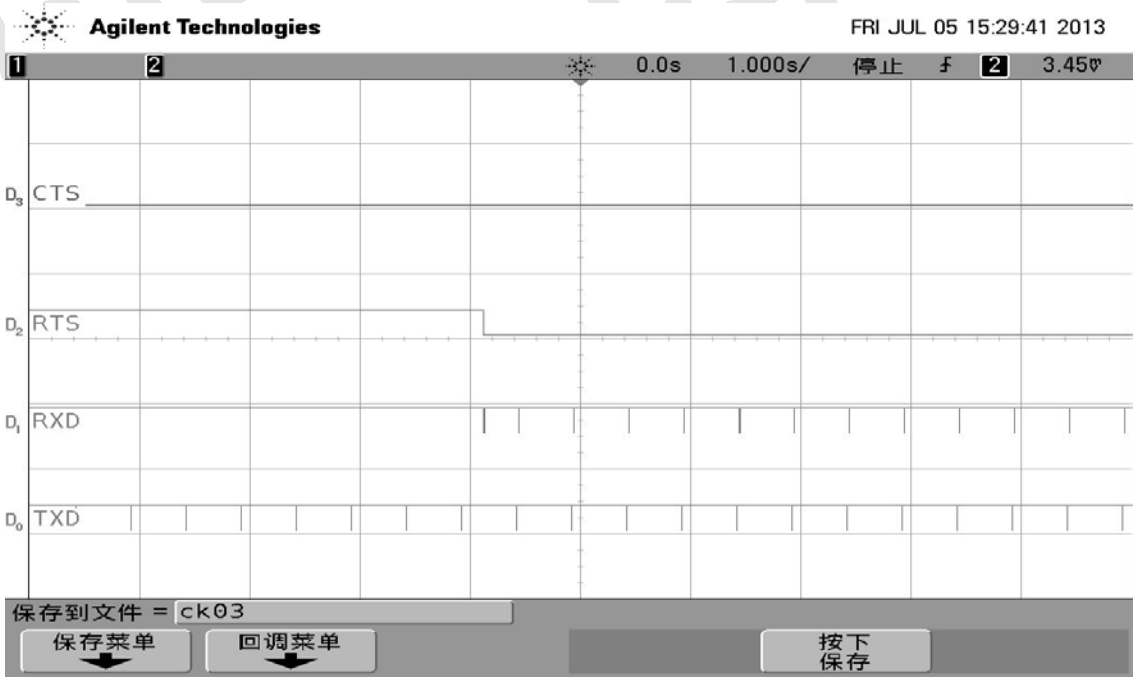

Figure 2-11 Wave Form

4. CTS_N output low level in IDLE mode and non-flow control mode by default.

5. CTS_N is the indicator signal of level cycles in flow control sleep mode.

The level cycles synchronized with the call signal of the module, the call period changed based on different base station, the formula of interval time:

4.615ms (TDMA frame duration) * 51 (number of frames) * DRX value

The parameter range of DRX (Discontinues Reception) is 2~9 (specified by network), the corresponding call interval time is 0.47-2.12 seconds.

The following figure shows the wave form of CTS_N When DRX=9:

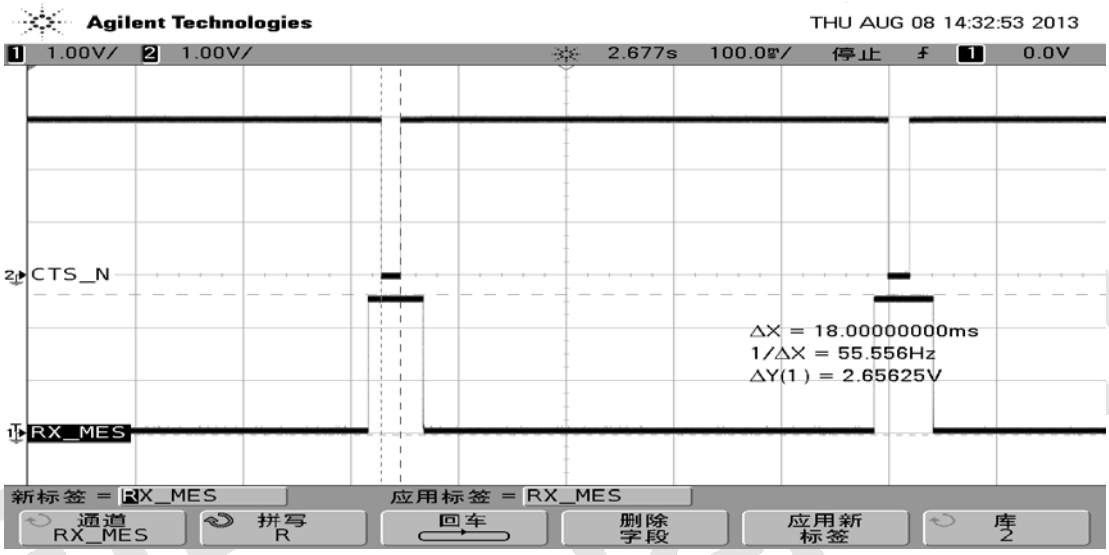

Figure 2-12 Wave Form

6. The UART data in different operating modes

(IDLE mode CTS is low, send AT&K3 and ATS24=2 command, the module goes into sleep mode, the value “2” means it automatically back to sleep mode after 2 seconds if there is no wake-up condition. When ATS24=2, after RXD_N send out the last data, module goes into sleep mode after 2s.

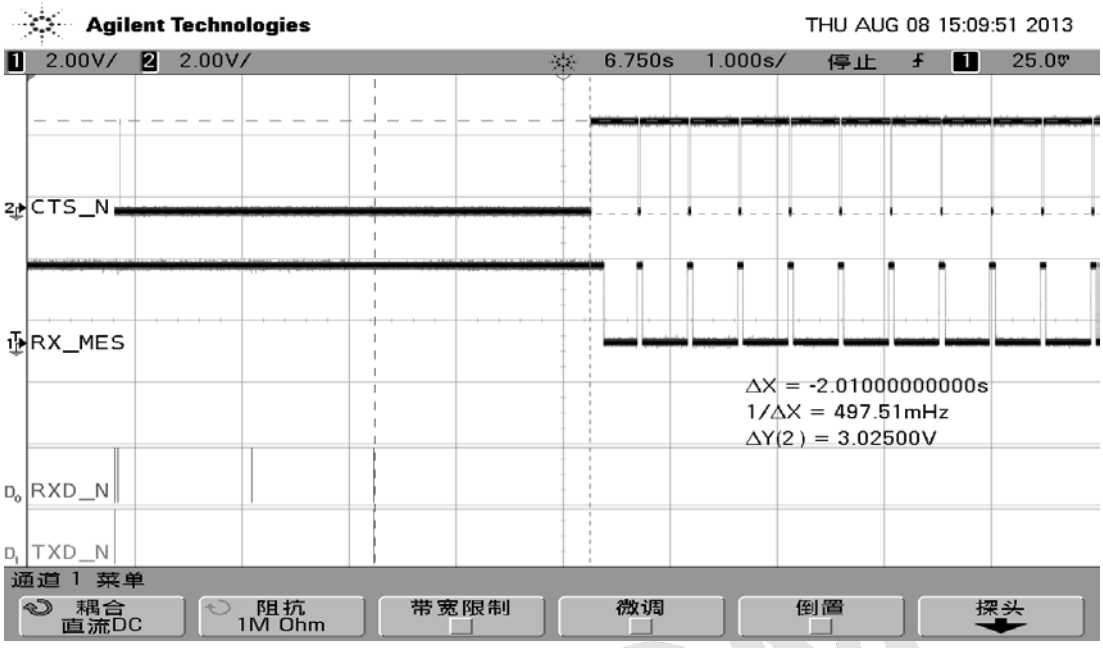

Figure 2-13 ATS24=2, module switches from IDLE mode to sleep mode after 2s

2.7.2 RING_N, DCD_N, DTR_N Control Signal

1. RING_N: In IDLE mode, RING_N outputs high level by default; when the base station call the module, RING_N outputs level change signal. As shown in the following figure, when the module receives a call, RING_N signal

Outputs 1S low level and 4S high level every 5S.

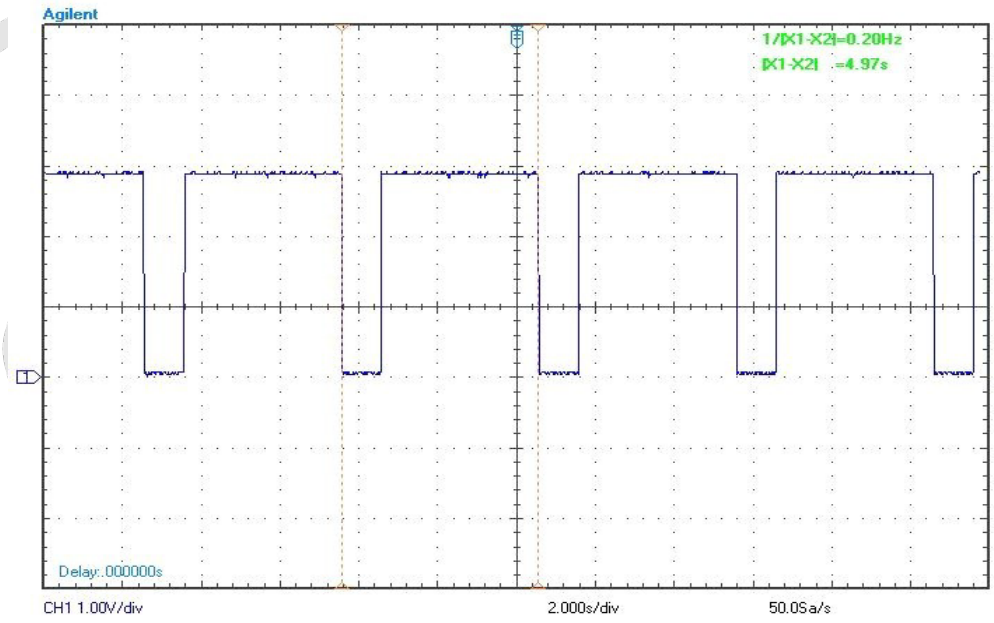

Figure 2-14 RING_N Wave Form

2. DCD_N outputs high level in IDLE mode: DCD_N signal is used for indicating CSD call or GPRS data

mode. For details, please refer to AT&C command in AT commands User Manual.

3. DTR_N, wake up module interrupt input, low level activated. Supports MCU GPIO controls module DTR, switch from sleep mode to idle mode.

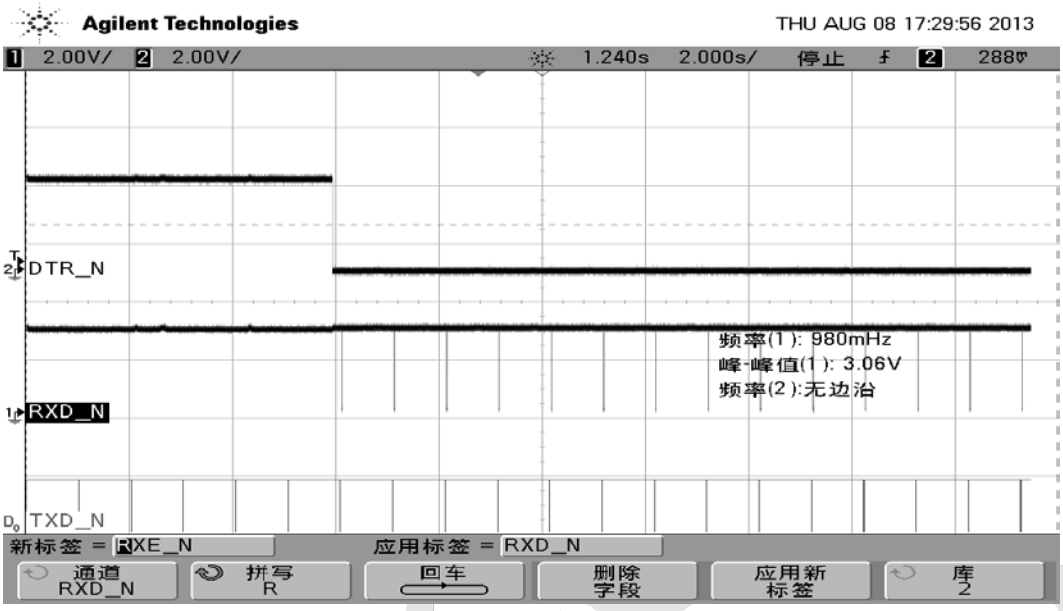

Figure 2-15 DTR wake up the module, RXD_N receives data

3 UART Software Design

The software configurations related to UART are: UART flow control, sleep mode and baud rate.

1. UART flow control AT commands:

“AT&K3” enable UART flow control

“AT&K0”disable UART flow control

2. Sleep mode AT commands:

“ATS24=3” The module goes into sleep mode after 3S.

“ATS24=0” The module exit from sleep mode.

3. Baud rate configuration:

“AT+IPR=n”

<Parameter>	**Description**	
<n><rate>	0	Auto baud rate
	1	600

<Parameter>	Description	
	2	1200
	3	2400
	4	4800
	5	9600
	6	19200
	7	38400
	8	57600
	9	Auto baud rate
	10	115200
	11	300
	12	230400
	13	460800
	14	921600
	15	14400
	16	28800
	The default value is auto-baud rate.	

Example:

AT+IPR=6
OK
AT+IPR?
+IPR: 19200
OK
AT+IPR=?
+IPR: (0-16,300,600,1200,2400,4800,9600,14400,19200,28800,38400,57600,115200,230400,460800,921600)
OK

For details, please refer to AT Commands User Manual.

4 Glossary

Name	Description
UART	Universal Asynchronous Receiver/Transmitter
DCE	Data Communications Equipment
RS-232C	Short for recommended standard-232C, a standard interface approved by the Electronic Industries Alliance (EIA) for connecting serial devices
DTR	Data terminal ready. Low level activated, it means the data terminal is ready, used when the module is in sleep mode, terminal wake up the module.
DSR	Data set ready. Low level activated, module is ready.
RTS	Request to send. Low level activated, terminal request module to send, it is used for determining module is in sending mode or not. (under flow control)
RI	Ring Indicator. Low level activated, notify terminal it's been called.
TXD	Transmitted data
RXD	Received data
DCD	Data Carrier Detect Module is connected to data link, notify DTE to receive data. When the module receive the data carrier signal from communication link, DCD signal is effective.